REMARKS

Claims 1-20 remain in the application.

Claims 1, 7, 17, and 19 are amended to more particularly point out and distinctly claim the subject matter of the claims.

Claims 2, 3, 6, and 8-16 are amended to provide proper antecedents to claims 1, 7, and 17.

35 USC 112 Rejection:

Claims 1-6, 12, 14, 19, and 20 were rejected under 35 USC 112 as being indefinite. The Office Action indicates that in claim 1 the phrases "deleting a first drive pulse" and the subsequent phrase "deleting the first drive pulse ...." in the next clause of claim 1 was confusing. Claim 1 is amended to move the phrase "in a second set" closer to the beginning of the third clause of claim 1 in order to eliminate the confusion for claim 1.

Also, claims 6, 12, and 19 were rejected for using the term re-insert and it was suggested to use the term "re-enable". However, the term re-insert is used in the specification and the term re-enabled is not used. Additionally, the term re-enabled is an incorrect characterization of the activities, and thus, the term re-insert remains in these claims. It is believed that this amendment to claim 1 now overcomes the 35 USC 112 rejection.

35 USC 102 rejection:

Claims 1-5, 7-11, 13, 17, and 18 were rejected under 35 U.S.C. 102 over U.S. patent no. 6,917,188 issued to Kernahan. This rejection is respectfully traversed. Amended claim 1 includes, among other things, organizing

output drive pulses of the power supply controller to into a plurality of sets with each set of the plurality of sets having a plurality of timing slots for the output drive pulses; deleting, in a second set, the first drive pulse from the first timing slot and a second drive pulse from a second timing slot; and reinserting into a fourth set a second number of deleted drive pulses. At least this combination of steps is not disclosed by the Kernahan reference.

The Office Action indicates, on page 3 in section 5, that Kernahan discloses "organizing output drive pulse of the power supply controller into a plurality of sets with each set of the plurality of sets having a plurality of time slots for the output drive pulses" and refers to column 54, lines 49-64, column 102, lines 19-28, and column 103, lines 50-65. Applicants respectfully submit that Kernahan does not organize the output drive pulses into sets. Kernahan uses a high-frequency clock and utilizes multiple cycles of the high-frequency clock as a timing signal to adjust the duty cycle of each drive pulse that is produced. However, Kernahan does not use the high-frequency clock to organize the drive pulses into sets having timing slots and does not remove the drive pulses from the timing slots within the set. Referring to FIG. 37 of Kernahan and column 49, lines 29-36, Kernahan discloses that each DPC frame may be divided into a plurality of counts of the high-frequency clock, and that the time between the counts determines the maximum PWM resolution that may be implemented. Also in conjunction with FIG. 37, note that column 24, lines 46-50, state that PFET pulse is the drive signal for operating the transistors of module 1202. Thus, the pulses of the high-frequency clock are dropped out in order to adjust the duty cycle or

on-time of the PFET pulse. Thus, the clock cycles of the high-frequency clock are used to form the DPC frame shown in FIG. 3 and the DPC frame is one cycle of the PFET signal. Kernahan does not disclose organizing all the PFET pulses or DPC frames into a plurality of sets as required by claim 1.

Additionally, Kernahan does not disclose that once the controller organizes the output drive pulses (PFET signals) into different sets that the controller should delete the first drive pulse from a first time slot of a first set and in a subsequent second set delete both the first drive pulse from the first time slot and a second drive pulse from a second time slot. Although Kernahan discloses implementing a cycle skipping operation, Kernahan does not disclose the combination of organizing the drive pulses into sets having specific timing slots and then removing specific pulses from specific timing slots. Kernahan discloses in column 67, lines 33-45, that "during the cycle skip mode a pulse may not be sent during the two (2) microsecond cycle (DPC frame). Instead, a pulse of fixed duration is sent in the MOS switch drive signals once every two or more cycles, such that the duty cycle averaged over the two or more cycles achieves the duty cycle necessary to maintain the output voltage within the control interval". Thus, Kernahan merely discloses not issuing drive pulses as long as the output voltage is not within the controlled level.

Further, Kernahan does not disclose reinserting into a third set a first number of deleted drive pulses into that third set, and subsequently reinserting a second number of deleted drive pulses into a fourth set. Kernahan merely discloses, in column 67, lines 46-51, that the duty cycle of the MOS switch drive signals are adjusted to restore the output voltage to the regulated voltage and the target.

Thus, Kernahan discloses changing the duty cycle of the drive signal to restore the output voltage and does not disclose reinserting missing drive pulses as is called for by claim 1, and certainly does not disclose using more that one set of drive pulses to re-insert deleted drive pulses. The method disclosed by Kernahan starts generating all drive pulses once the output voltage reaches the desired (target) value. Accordingly, it is respectfully submitted that, when these limitations of claim 1 are viewed as a whole, the Kernahan reference can not anticipate amended claim 1.

Claims 2-5 depend from claim 1 and are believed to be allowable for at least the same reasons as claim 1.

Additionally, claim 4 includes forming each set with a same number of timing slots. Since Kernahan does not disclose organizing the drive pulses into sets, Kernahan can not disclose forming the sets with the same number of timing slots.

Also, claim 5 includes forming each set with a different number of timing slots. Forming sets with different numbers of timing slots is not disclosed by Kernahan.

For these reasons, it is respectfully submitted that Kernahan is deficient in anticipating claims 2-5.

Amended claim 7 includes, among other elements, forming the power supply controller to organize output drive pulses into a plurality of sets with each set having a plurality of timing slots for the output drive pulses; forming the power supply controller to delete a first number of drive pulses in a first set; and forming the power supply controller to delete in a second set both the first number of drive pulses

plus a second number of drive pulses. As explained in the traversal of the 35 USC 102 rejection of claim 1, Kernahan does not organize the output drive pulses into sets having a plurality of timing slots. Also, Kernahan does not disclose deleting a first number of drive pulses from a respective first number of timing slots in the first set; and in a subsequent second set delete an additional second number of drive pulses from a respective second number of timing slots. When claim 7 is viewed as a whole, at least these steps of claim 7 are not disclosed by Kernahan. Accordingly, it is respectfully submitted that Kernahan can not anticipate amended claim 7.

Claims 8-11 depend from claim 7 and are believed to be allowable for at least the same reasons as claim 7.

Additionally, claim 8 includes delete a first drive pulse from a first timing slot and a second drive pulse from a second timing slot. Since Kernahan does not form the drive pulses into sets, Kernahan can not delete the specific drive pulses from specific timing slots within the set.

Also, claim 10 includes forming the power supply controller to form each set with sixteen timing slots. Kernahan does not disclose forming the drive pulses into sets having sixteen timing slots within the set.

Further, claim 11 includes forming the power supply controller to form each set with a different number of timing slots. Using sets with different numbers of timing slots for the drive pulses is not disclosed by Kernahan.

Amended claim 17 includes, among other features, a control block coupled to organize drive pulses to the output transistor into a plurality of sets having a plurality of

timing slots; ..... a control signal to delete a first drive pulse in a first set of the plurality of sets from a first timing slot ..... and to increase the number of deleted drive pulses from each successive set of the plurality of sets so that each successive set has deleted more drive pulses from respective timing slots than an immediately prior set.

Kernahan does not disclose deleting a first drive pulse from a first timing slot of a first set and in subsequent sets increasing the number of drive pulses deleted from timing slots. Accordingly, it is respectfully submitted that claim 17 can not be anticipated by the Kernahan reference.

Claims 18-20 depend from claim 17 and are believed to be allowable for at least the same reasons as claim 17.

35 USC 103 rejection:

Claims 6, 12, 14, 19, and 20 were rejected under 35 U.S.C. 103 over Kernahan in view of U.S. patent no. 5,747,977 issued to Hwang. This rejection is respectfully traversed.

Claim 6 depends from claim 1 and includes all the limitations of claim 1. The deficiencies of Kernahan relative to claim 1 are discussed in the traversal of the 35 USC 102 rejection of claim 1 which is incorporated herein by reference. Additionally, claim 6 includes re-inserting the first drive pulse into the first timing slot. Since the set has the first timing slot, a pulse can be re-inserted back into that first space or slot in the set.

Hwang does not teach or suggest grouping drive pulses into a plurality of sets having timing slots for the drive

pulses. Thus, Hwang can not make for the deficiencies of Kernahan relative to this element of claim 1 and claim 6. The Office Action states that Hwang re-enables pulses once the load rises above the light load threshold. Please note that in column 6, lines 47-53, Hwang teaches re-enabling all drive pulses and does not re-insert drive pulses back into timing slots of the set. Accordingly, it is respectfully submitted that the combination of Hwang with Kernahan can not make claim 6 obvious.

Claims 12 and 14 depend from claim 7 and includes all the limitations of claim 7. The deficiencies of Kernahan relative to claim 7 are discussed in the traversal of the 35 USC 102 rejection of claim 7 which is incorporated herein by reference.

Additionally, claim 12 includes, re-insert at least one deleted drive pulse into a third set. The combination of Hwang and Kernahan merely teaches that the generation of all drive pulses should be re-enabled. The combined references do not teach or suggest re-inserting drive pulses back into specific timing slots of sets.

Claim 14 includes, sequentially increase the number of re-inserted drive pulse for each set subsequent to the third set. The combined references do not teach or suggest sequentially increasing the number of drive pulses re-inserted into timing slots for subsequent sets. Accordingly, it is respectfully submitted that claims 12 and 14 are not made obvious by the combined relied on references.

Claims 19 and 20 depend from claim 17 and include all the limitations of claim 17. The deficiencies of Kernahan

relative to claim 17 are discussed in the traversal of the 35 USC 102 rejection of claim 17 which is incorporated herein by reference. Combining Hwang with Kernahan does not make-up for theses deficiencies of Kernahan. Accordingly, it is respectfully submitted that the combined relied on references are deficient in making claims 12 and 14 obvious.

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CONCLUSION

Applicant(s) made an earnest attempt to place this case in condition for allowance. In view of all of the above, it is believed that the claims are allowable, and that the case is now in condition for allowance, which action is earnestly solicited.

Although it is believed that no fees are due for this amendment, the Commissioner is hereby authorized to charge any fees that may be required or credit any overpayment to Deposit Account 50-1086.

If there are matters which can be discussed by telephone to further the prosecution of this Application, the Examiner is invited to call the undersigned attorney at the Examiner's convenience.

Respectfully submitted,
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